

Fig.1

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Link Training
State Machine

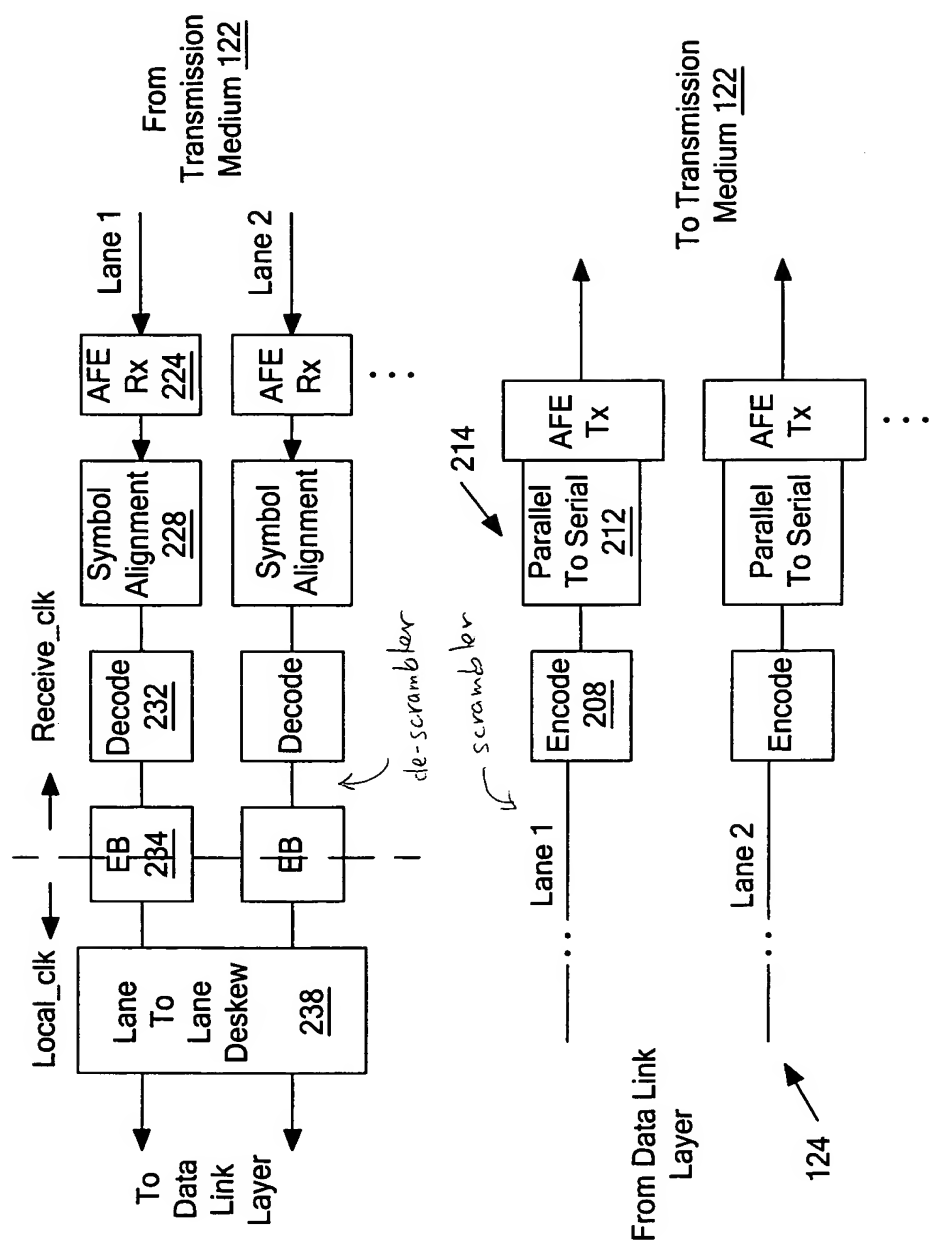


Fig.2

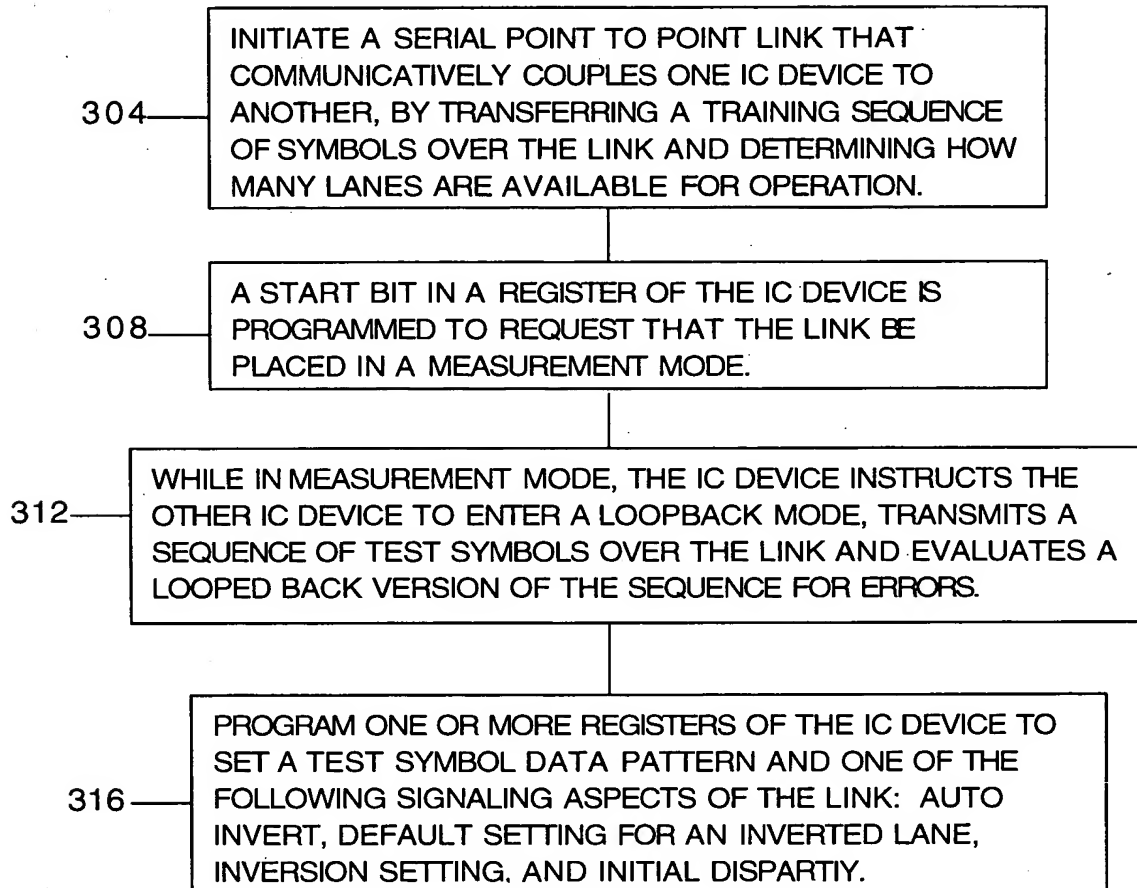


FIG. 3

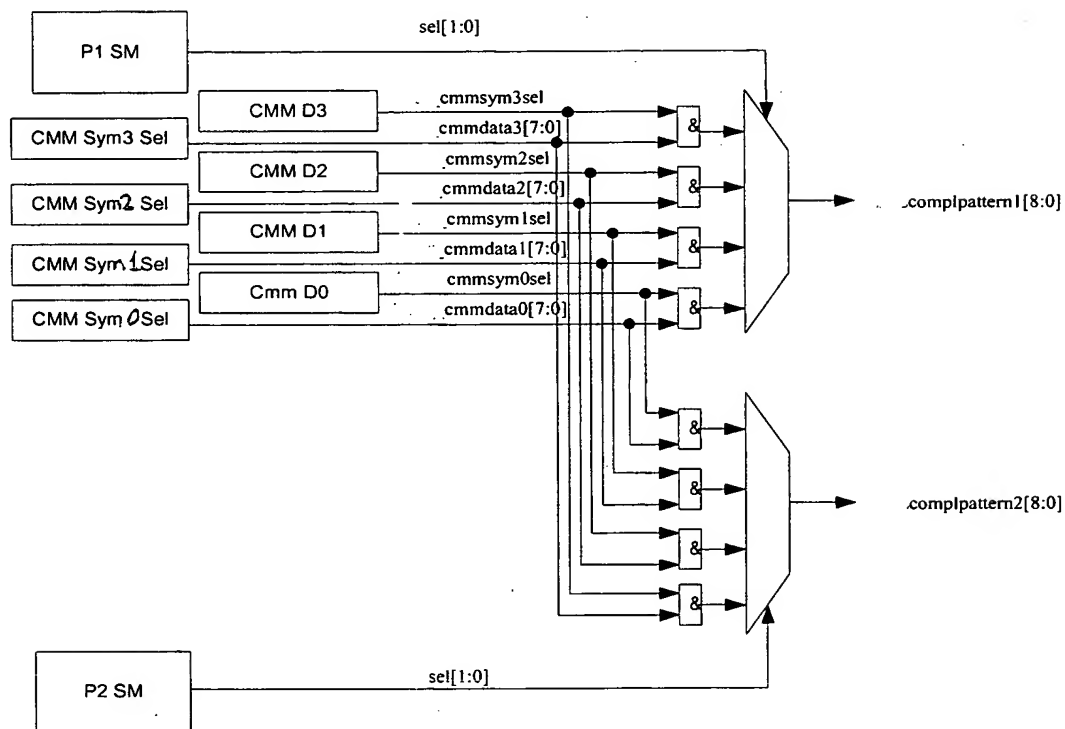


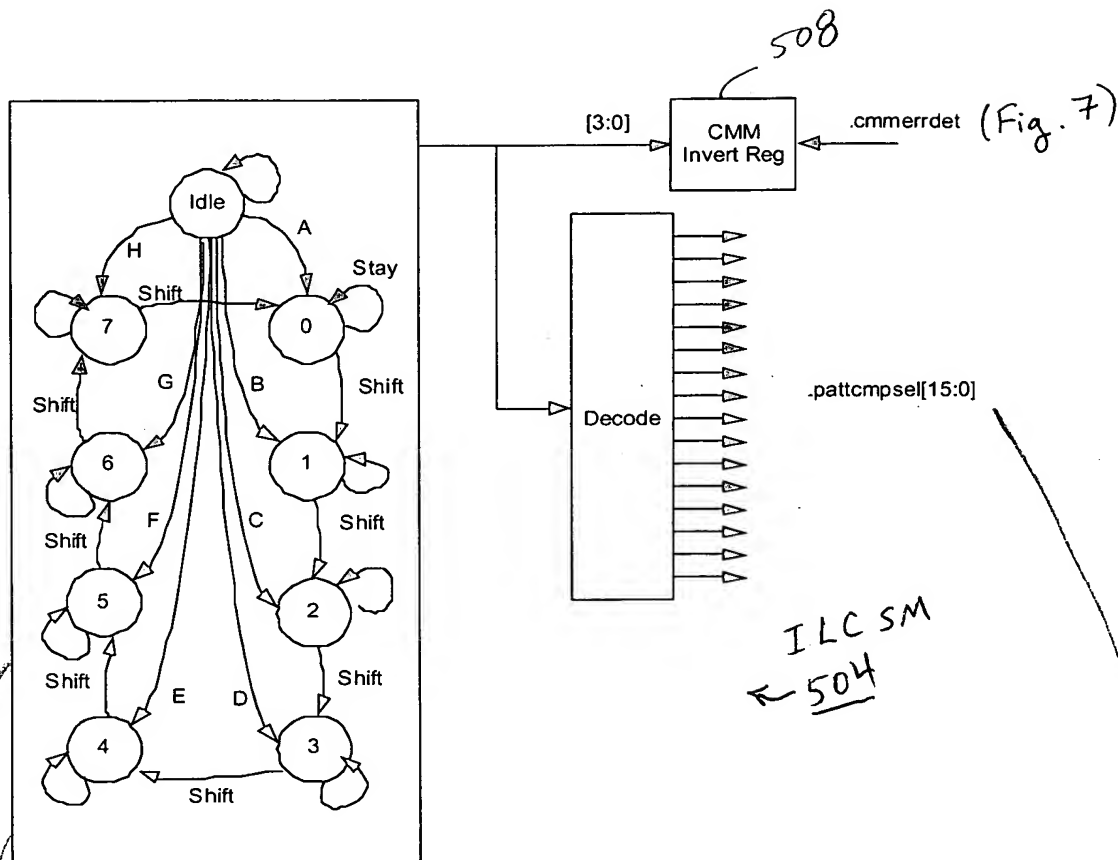
Fig. 4A

Register	D0	D1	D2	D3	D0	D1
Symbol	K23.5	D21.5	K23.5	D10.2	K23.5	D21.5
Disparity	0	1	1	0	0	1
Pattern	0011111010	1010101010	1100000101	0101010101	00111111010	1010101010

Fig. 4B

Register	D0	D0	D0	D1	D2	D3	D0	D0
Symbol	K23.5	K23.5	K23.5	D21.5	K23.5	D10.2	K23.5	K23.5
Disparity	0	1	0	1	1	0	0	1
Pattern	001111101	1100000101	0011111010	1010101010	1100000101	0101010101	0011111010	1100000101

Fig. 4C



Shift : CMM Auto Invert
 Stay : CMM Auto Invert

= 1
 = 0

A : CMM Invert Enable
 B : CMM Invert Enable
 C : CMM Invert Enable
 D : CMM Invert Enable
 E : CMM Invert Enable
 F : CMM Invert Enable
 G : CMM Invert Enable
 H : CMM Invert Enable

And CMM Invert Lane Number
 And CMM Invert Lane Number
 And CMM Invert Lane Number
 And CMM Invert Lane Number
 And CMM Invert Lane Number
 And CMM Invert Lane Number
 And CMM Invert Lane Number
 And CMM Invert Lane Number
 =000
 =001
 =010
 =011
 =100
 =101
 =110
 =111

State	pattcmpsel[0:15]
Idle	0000000000000000
0	1000000010000000
1	0100000001000000
2	0010000000100000
3	0001000000010000
4	0000100000001000
5	0000010000000100
6	0000001000000010
7	0000000100000001

Fig. 5

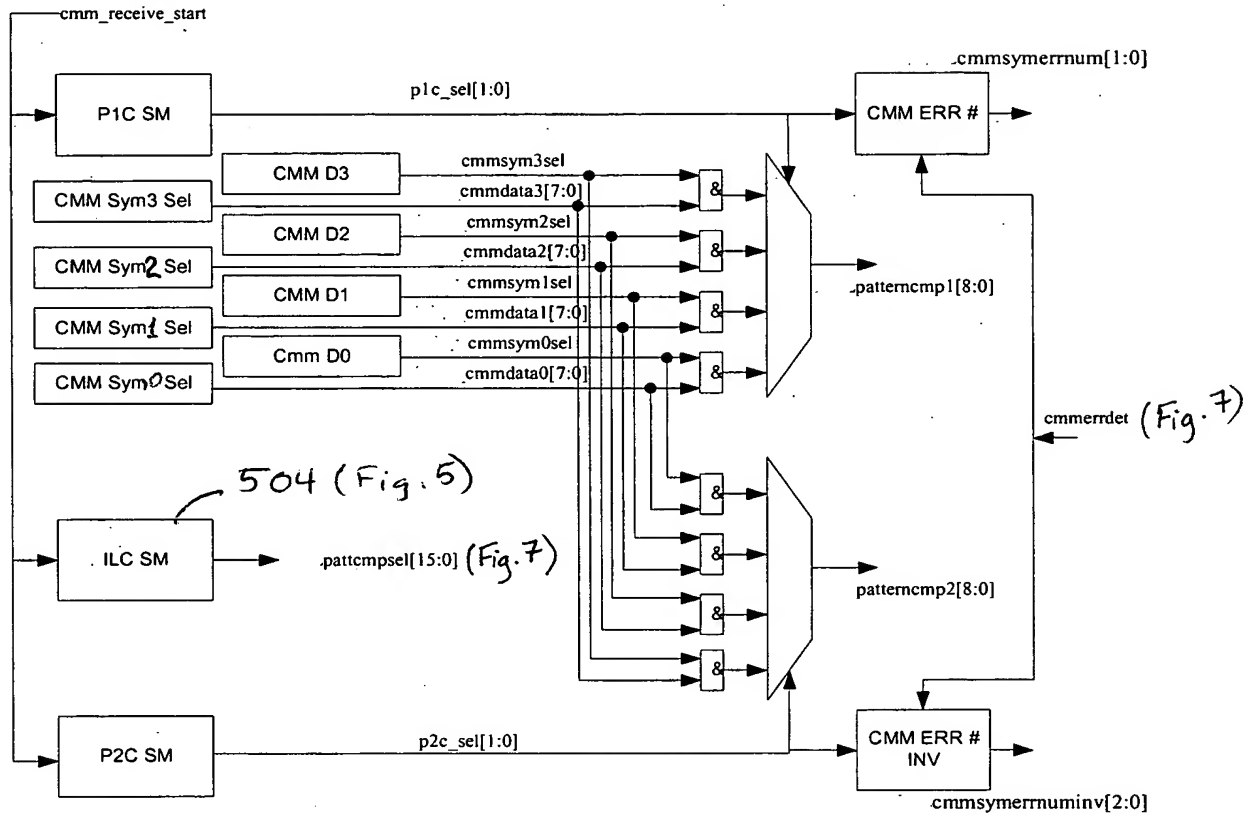


Fig. 6

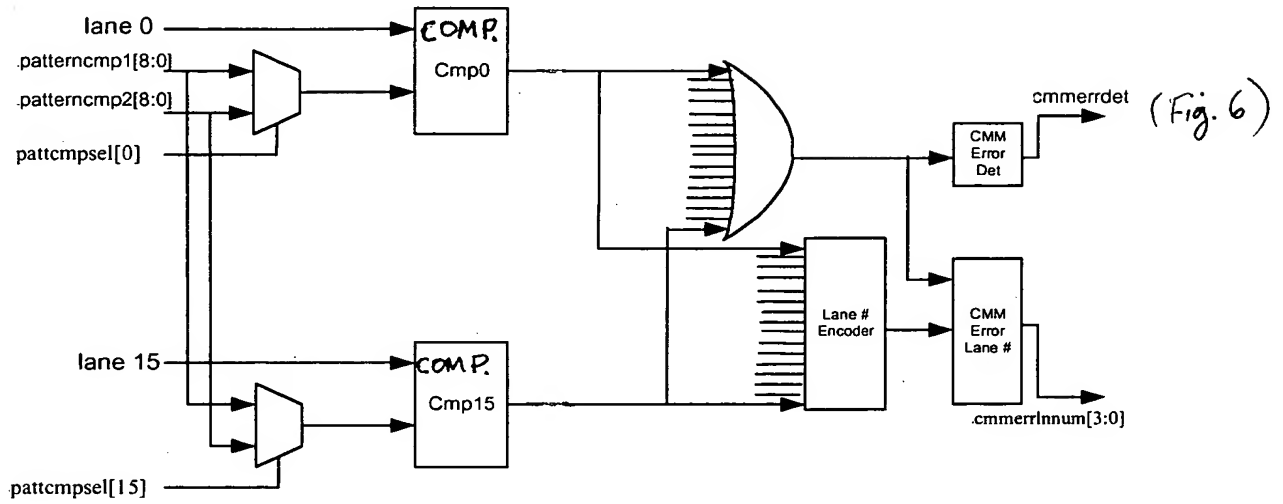


Fig. 7

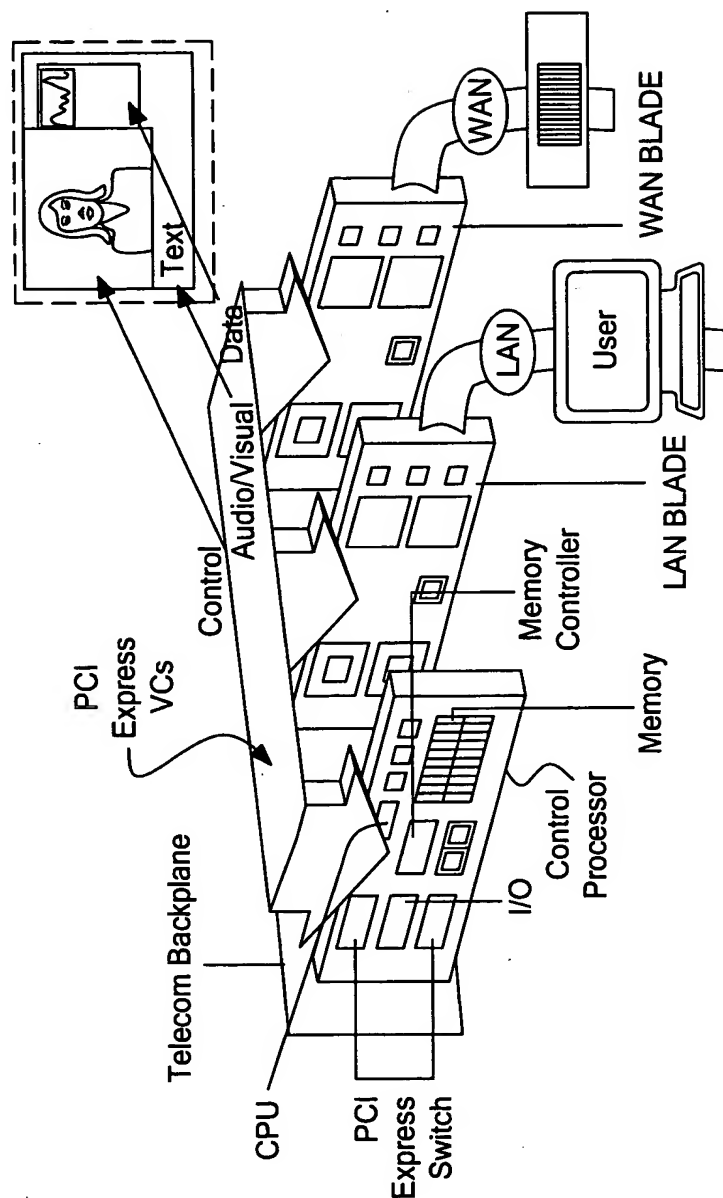


Fig.8

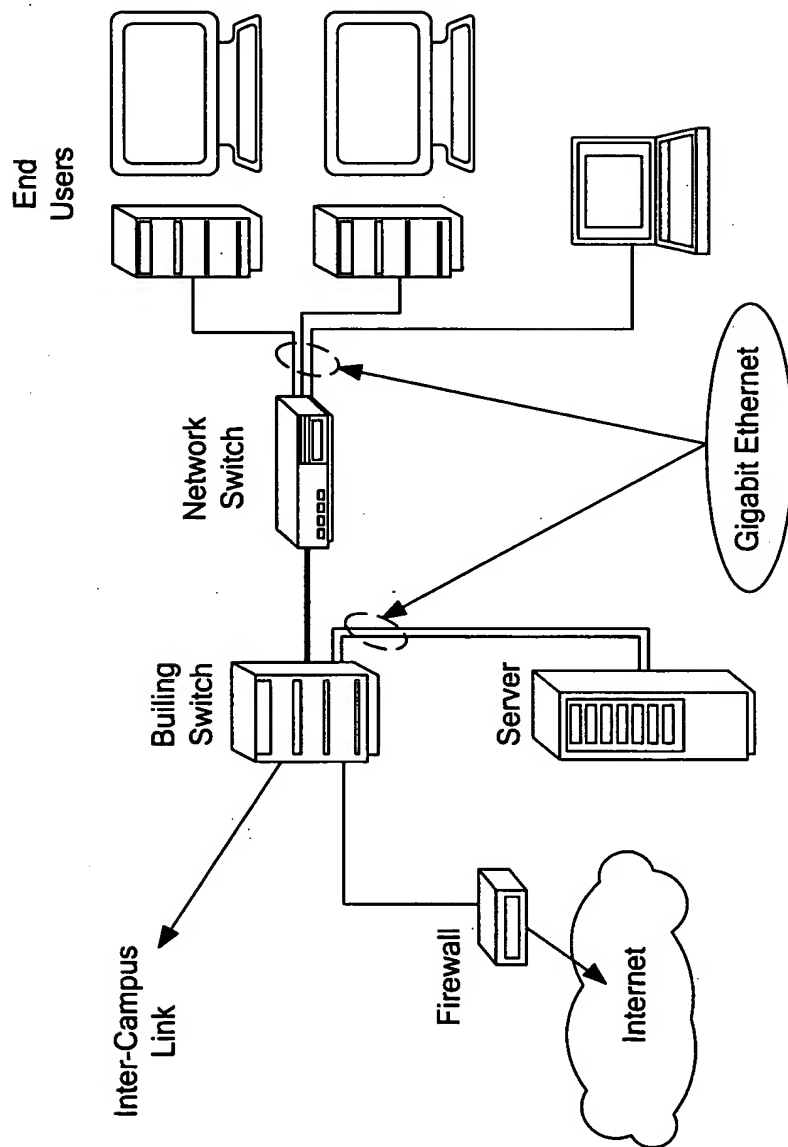


Fig.9